L Number	Hits	Search Text	DB	Time stamp
1	2370	(sloped or taper$3) near3 via	USPAT; US-PGPUB	2004/08/24 08:49
2	98	((sloped or taper$3) near3 via) and (back near3 (chip or substrate or wafer))	USPAT; US-PGPUB	2004/08/24 08:56
3	71	(((sloped or taper$3) near3 via) and (back near3 (chip or substrate or wafer))) and @ad<20011220	USPAT; US-PGPUB	2004/08/24 08:48
4	10	((((sloped or taper$3) near3 via) and (back near3 (chip or substrate or wafer))) and @ad<20011220) and isotropic	USPAT; US-PGPUB	2004/08/24 08:56
5	1083	(sloped or taper$3) near3 via	EPO; JPO; DERWENT; IBM_TDB	2004/08/24 08:49
6	2	((sloped or taper$3) near3 via) and (back near3 (chip or substrate or wafer))	EPO; JPO; DERWENT; IBM_TDB	2004/08/24 08:49
7	1034	438/667,668,673,928,978.ccls.	USPAT; US-PGPUB	2004/08/24 08:58
8	864	438/667,668,673,928,978.ccls. and @ad<20011220	USPAT; US-PGPUB	2004/08/24 08:59
9	166	(438/667,668,673,928,978.ccls. and @ad<20011220) and (back near3 (chip or substrate or wafer))	USPAT; US-PGPUB	2004/08/24 08:59
10	19	((438/667,668,673,928,978.ccls. and @ad<20011220) and (back near3 (chip or substrate or wafer))) and isotropic	USPAT; US-PGPUB	2004/08/24 08:59
11	2503	257/774-776.ccls.	USPAT; US-PGPUB	2004/08/24 08:59
12	2023	257/774-776.ccls. and @ad<20011220	USPAT; US-PGPUB	2004/08/24 08:59
13	128	(257/774-776.ccls. and @ad<20011220) and (back near3 (chip or substrate or wafer))	USPAT; US-PGPUB	2004/08/24 08:59
14	128	((257/774-776.ccls. and @ad<20011220) and (back near3 (chip or substrate or wafer))) not (((438/667,668,673,928,978.ccls. and @ad<20011220) and (back near3 (chip or substrate or wafer))) and isotropic)	USPAT; US-PGPUB	2004/08/24 08:59
15	16	(((257/774-776.ccls. and @ad<20011220) and (back near3 (chip or substrate or wafer))) not (((438/667,668,673,928,978.ccls. and @ad<20011220) and (back near3 (chip or substrate or wafer))) and isotropic)) and isotropic	USPAT; US-PGPUB	2004/08/24 09:06
16	1	("6184060").PN.	USPAT; US-PGPUB	2004/08/24 09:38
17	126	(two adj sided) with etching	USPAT; US-PGPUB	2004/08/24 09:47
18	62	((two adj sided) with etching) and via	USPAT; US-PGPUB	2004/08/24 09:39
19	51	(((two adj sided) with etching) and via) and @ad<20011220	USPAT; US-PGPUB	2004/08/24 09:48
20	73	(one adj sided) with etching	USPAT; US-PGPUB	2004/08/24 09:47
21	63	((one adj sided) with etching) and @ad<20011220	USPAT; US-PGPUB	2004/08/24 09:48
22	58	(((one adj sided) with etching) and @ad<20011220) not ((((two adj sided) with etching) and via) and @ad<20011220)	USPAT; US-PGPUB	2004/08/24 10:40
23	1214	(DRIE or (deep adj reactive adj ion adj etching))	USPAT; US-PGPUB	2004/08/24 10:41
24	670	((DRIE or (deep adj reactive adj ion adj etching))) and @ad<20011220	USPAT; US-PGPUB	2004/08/24 10:41
25	567	(((DRIE or (deep adj reactive adj ion adj etching))) and @ad<20011220) and (wafer or substrate or chip)	USPAT; US-PGPUB	2004/08/24 10:41

26	131	((((DRIE or (deep adj reactive adj ion adj etching))) and @ad<20011220) and (wafer or substrate or chip)) and (sloped or tapered)	USPAT; US-PGPUB	2004/08/24 11:01
27	365	((((DRIE or (deep adj reactive adj ion adj etching))) and @ad<20011220) and (wafer or substrate or chip)) and (via or groove)	USPAT; US-PGPUB	2004/08/24 11:01

US-PAT-NO: 6662419

DOCUMENT-IDENTIFIER: US 6662419 B2

TITLE: Method for fabricating film bulk acoustic resonators to achieve high-Q and low loss

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Detailed Description Text - DETX (6):
FIGS. 5A and 5B illustrate top and side views respectively of the substrate 300 after a portion of the substrate material beneath the piezoelectric layer and the seed layer 310 have been removed. Removing a portion of the substrate 300 produces an opening 500 on the back side of the substrate. The substrate material 300 that is removed corresponds to the portion of the substrate 300 which is under the active area of the final device or FBAR. The substrate material is removed using deep-trench reactive-ion etching (**DRIE**). The etched profile of the **DRIE** is adjusted to be negative so as to produce a first sloped sidewall 502 and a second sloped sidewall 504.

Detailed Description Text - DETX (7):
FIGS. 6A and 6B illustrate the substrate after a portion of the seed layer 310 beneath the piezoelectric film 410 has been removed. The single crystal seed layer 310 is etched from the back side of the wafer through the previously etched **DRIE** window or opening 500 formed when the substrate material 300 was removed from the back side of the wafer. The etch for removing the single crystal seed layer 310 is self aligned and is stopped on the piezoelectric layer 410 by end point detection. More specific, the etch

for removing the single crystal seed layer 310 stops at or near the first surface 412 of the piezoelectric layer 410. The etch to remove the single crystal seed layer 310 exposes the piezoelectric layer 410 and specifically surface 412 along the back side of the substrate. This etch can be said to form a second window 600 which is bounded by the single crystal seed layer 310 and exposes the surface 412 of the piezoelectric crystal 410 at the back side of the substrate 300.

Detailed Description Text - DETX (8):
FIGS. 7A and 7B show top and side views of the substrate after a second portion 700 of the first electrode is deposited on the first surface 412 of the piezoelectric film 410. The bottom electrode metal is deposited from the back side of the wafer. Depositing metal from the back side of the wafer or substrate 300 produces the second portion 700 of the first electrode. The back side surface of the substrate 300 is also metallized as is shown by metal layers 710 and 712 in FIG. 7B. The second electrode 700 makes electrical contact with the first portion of the first electrode 400 or what is also known as the buried metal trace. It should be noted that there is no metal deposited on the sidewalls of the opening 500. When the opening 500 was made, the **DRIE** was adjusted to be negative thereby producing sloping sidewalls 502 and 504. When the metal layer is deposited which forms the second portion 700 of the first electrode, the sloped sidewalls prevent deposit of metal on the sidewalls 502, 504. This prevents a continuous metal layer being formed over all the bulk silicon substrate 300 and provides for a separate electrode 700 which covers most of the first surface 412 of the piezoelectric film 410. It should

be noted that the first portion 400 of the first electrode and the second portion 700 of the first electrode form the first electrode. Typically the second portion 700 of the first electrode overlaps the first portion 400 of the first electrode by an amount to provide adequate electrical connection between the first portion 400 and the second portion 700 of the first electrode. As shown, the overlapping is approximately 10 micrometers.

Detailed Description Text - DETX (11):

FIGS. 10A and 10B illustrate the substrate 800 after a portion of the substrate material beneath the piezoelectric film 910 has been removed. As best illustrated by FIG. 10B, the silicon substrate under piezoelectric film 910 is removed using deep-trench reactive-ion etching (**DRIE**). Removing a portion of the silicon substrate 800 from the back side of the substrate 800, produces an opening 1000. The opening 1000 can also be termed a **DRIE** etch window. The etch profile of the **DRIE** window or opening 1000 is adjusted to be negative. The negative etched profile of the opening or **DRIE** window 1000 produces a first sloped sidewall 1002 and a second sloped sidewall 1004.

Detailed Description Text - DETX (12):

FIGS. 11A and 11B illustrate the substrate or the device after a portion of the seed layer beneath the piezoelectric material or beneath the piezoelectric film 910 has been removed. The nonconductive seed layer 810 is etched or removed from the back side of the substrate through the previously etched **DRIE** window or opening 1000. The etch is self aligned and effectively stops on the piezoelectric layer 910 by end point detection. Specifically, the etch stops at or near the first surface 912 of the piezoelectric layer

or film 910. The result of the etch from the back side that removes the nonconductive seed layer 810 is an opening 1100 in the seed layer 810. The opening 1100 exposes surface 912 of the piezoelectric film or layer 910 as well as part of the portion 1214 of the first portion 1210 of the first electrode.

Detailed Description Text - DETX (13):

FIGS. 12A and 12B illustrate top and side views, respectively, of the substrate after the back side of the substrate 800 is metallized. Metal is deposited on the back side of the wafer. The deposited metal form the second portion 1212 of the first electrode 1200 as well as metallized layers 1220 and 1222 on the back side of the substrate 800. The opening 1000 or **DRIE** window which was previously adjusted to have a negative profile and to produce sloping sidewalls 1002 and 1004 prevents deposit of the metal on the sidewalls 1002, 1004. This in turn prevents a continuous metal layer being formed on the bulk silicon substrate so that the second portion 1212 of the first electrode 1200 is separated from the other metallized portions 1220 and 1222. The second portion 1212 of the first electrode 1200 contacts the first portion 1210 of the first electrode. The first portion 1210 and the second portion 1212 of the first electrode 1200 overlap so that electrical contact is made between the first and second portions. In this particular embodiment, the overlap is approximately 12 micrometers.

Detailed Description Text - DETX (17):

As best seen in FIG. 15B, the silicon substrate 1300 beneath the piezoelectric film 1410 has been removed by deep-trench reactive-ion etching (**DRIE**). Removal of the substrate portion beneath the

US-PAT-NO: 6723250

DOCUMENT-IDENTIFIER: US 6723250 B1

TITLE: Method of producing structured wafers

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Detailed Description Text - DETX (2):
FIG. 1 shows a first embodiment of the method according to the present invention as a **two-sided** one-step **etching** process. Part 1 shows a cross-sectional view of wafer 20, which made be made of a single material, with a front side 22, a back side 23 and an edge area 21. The wafer is shown only partially, continuing toward the left, where it is delimited by another edge area (not shown). A nitride layer is applied to the wafer by gas phase deposition. Then the nitride layer is structured by a conventional photoresist technique, with the resist being applied to the nitride layer, exposed selectively and then developed; (when using a positive resist) the exposed part of the resist is next removed, then the exposed part of the nitride layer is removed, usually by a plasma etching process, and finally the remaining unexposed part of the resist is removed, e.g., by ashing the resist in an oxygen plasma. Nitride structuring is performed first on the front side of the wafer, as shown in Part 1; this structuring yields structured nitride layer 25. Unstructured nitride layer 24 is still imaged on the back side.

Detailed Description Text - DETX (5):
The wafer with the structure illustrated in Part 8 is

then exposed to a wet chemical etching process in a KOH bath. First the wafer is pre-etched in the area of through hole 29 to be formed later, in order to partially remove the silicon and produce recesses 42 on both sides (see Part 9). Then thin oxide layer 41 is removed in subregion 40 with a hydrofluoric acid etchant medium which attacks all areas of the silicon dioxide layer in the immersion bath; however, since the oxide layer in subregion 40 is thinner than the remaining layer, it can be removed completely selectively with respect to the remaining oxide layer in subregion 40 if the etching process with the hydrofluoric acid etchant medium is terminated as soon as thin oxide layer 41 is removed (Part 10). Finally, the wafer is etched in KOH until the silicon is removed to the final etching depths. Part 11 shows the structured wafer after subsequent removal of the passivation layer; it has a through hole 29 and a shallow cavern 43. A structuring of the wafer has been achieved through the procedure of a **two-sided** two-step KOH **etching** process illustrated in FIG. 2 in comparison with FIG. 1, resulting in a cavern 43 which is shallower than cavern 28 from FIG. 1.

US-PAT-NO: 6517402

DOCUMENT-IDENTIFIER: US 6517402 B1

TITLE: Plasma addressed liquid crystal display with etched glass spacers

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Detailed Description Text - DETX (10):

Two preferred ways for etching the glass to make the hole walls as close to the vertical as possible are described in FIGS. 6 and 7 of the fourth referenced related application, whose contents are incorporated herein. In brief, this can be done as **one-sided etching** with an etch mask on one surface of the spacer plate and with relatively small openings in the etch mask and **etching** holes whose lateral dimensions are at least five times larger than the mask opening and the depth of the hole, in this case the thickness of the sheet 50. Using an isotropic etchant during the etching process, as the etching progresses, the sidewalls become steeper. The larger the lateral dimensions of the etched hole relative to the thickness of the glass sheet 50, the steeper the sidewalls. As an example, not meant to be limiting, for a glass sheet 50 of about 100 .mu.m thick, to etch holes that are 500 .mu.m wide, the mask hole is preferably 100 .mu.m wide. For a panel with straight channels as illustrated in FIG. 2, the holes 52 would be elongated slots extending nearly the full length of the plate 50, but would terminate at opposite sides in an annular glass border region 53 so that the plate 50 remains as an integral element except for the holes 52 in the form of parallel

slots spaced apart by
spacer walls 58.